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Min, B.; Choi, G.;
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Byeong Min; Gwan Choi;
Dependable Computing, 2001. Proceedings. 2001 Pacific Rim International Symposium on , 17-19 Dec. 2001
Pages:183 - 190

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1 Regression-based RTL power modeling

Alessandro Bogliolo, Luca Benini, Giovanni De Micheli

July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(391.65 KB) Additional Information: full citation, abstract, references, citings, index terms

Register-transfer level (RTL) power estimation is a key feature for synthesis-based design flows. The main challenge in establishing a sound RTL power estimation methodology is the construction of accurate, yet efficient, models of the power dissipation of functional macros. Such models should be automatically built, and should produce reliable average power estimates. In this paper we propose a general methodology for building and tuning RTL power models. We address both hard macros (presy ...

Keywords: RTL design, RTL power modeling, adaptive characterization, functional macros, regression models

2 Property-Specific Testbench Generation for Guided Simulation

Aarti Gupta, Albert E. Casavant, Pranav Ashar, Akira Mukaiyama, Kazutoshi Wakabayashi, X. G. (Sean) Liu

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(208.21 KB) Publisher Site Additional Information: full citation, abstract

Simulation continues to be the primary technique for functional validation of designs. It is important that simulation vectors be effective in targeting the types of bugs designers expect to find rather than some generic coverage metrics. The overall focus of our work is to generate a property-specific testbench for guided simulation, that is targeted either at proving the correctness of a property or at finding a bug. This is facilitated by generation of a property-specific model, called a "Wit ...

Keywords: guided simulation, intelligent testbench generation, witness graph, property-specific testbench, symbolic model checking, approximate model checking, iterative refinement

3 Integrating performance monitoring and communication in parallel computers

Margaret Martonosi, David Ofelt, Mark Heinrich

May 1996 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1996 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 24 Issue 1

Full text available: pdf(1.49 MB) Additional Information: full citation, abstract, references, citings, index terms

A large and increasing gap exists between processor and memory speeds in scalable cache-coherent multiprocessors. To cope with this situation, programmers and compiler writers must increasingly be aware of the memory hierarchy as they implement software. Tools to support memory performance tuning have, however, been hobbled by the fact that it is difficult to observe the caching behavior of a running program. Little hardware support exists specifically for observing caching behavior; furthermore ...

4 Piranha: a scalable architecture based on single-chip multiprocessing

Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(191.10 KB) Additional Information: full citation, abstract, references, citings, index terms

The microprocessor industry is currently struggling with higher development costs and longer design times that arise from exceedingly complex processors that are pushing the limits of instruction-level parallelism. Meanwhile, such designs are especially ill suited for important commercial applications, such as on-line transaction processing (OLTP), which suffer from large memory stall times and exhibit little instruction-level parallelism. Given that commercial applications constitute by fa ...

5 Process migration

September 2000 **ACM Computing Surveys (CSUR)**, Volume 32 Issue 3

Full text available: pdf(1.24 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Process migration is the act of transferring a process between two machines. It enables dynamic load distribution, fault resilience, eased system administration, and data access locality. Despite these goals and ongoing research efforts, migration has not achieved widespread use. With the increasing deployment of distributed systems in general, and distributed operating systems in particular, process migration is again receiving more attention in both research and product development. As hi ...

Keywords: distributed operating systems, distributed systems, load distribution, process migration

6 The performance impact of flexibility in the Stanford FLASH multiprocessor

Mark Heinrich, Jeffrey Kuskin, David Ofelt, John Heinlein, Joel Baxter, Jaswinder Pal Singh, Richard Simoni, Kourosh Gharachorloo, David Nakahira, Mark Horowitz, Anoop Gupta, Mendel Rosenblum, John Hennessy

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29 , 28 Issue 11 , 5

Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, references, citings, index terms

A flexible communication mechanism is a desirable feature in multiprocessors because it allows support for multiple communication protocols, expands performance monitoring

capabilities, and leads to a simpler design and debug process. In the Stanford FLASH multiprocessor, flexibility is obtained by requiring all transactions in a node to pass through a programmable node controller, called MAGIC. In this paper, we evaluate the performance costs of flexibility by comparing the performance of ...

7 A two-state methodology for RTL logic simulation
Lionel Bening
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(51.47 KB) Additional Information: full citation, references, index terms

Keywords: 2-state, RTL, X-state, initialization, optimism, pessimism, random, simulation

8 The Stanford FLASH multiprocessor
J. Kuskin, D. Ofelt, M. Heinrich, J. Heinlein, R. Simoni, K. Gharachorloo, J. Chapin, D. Nakahira, J. Baxter, M. Horowitz, A. Gupta, M. Rosenblum, J. Hennessy
April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture**, Volume 22 Issue 2
Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, citings, index terms

The FLASH multiprocessor efficiently integrates support for cache-coherent shared memory and high-performance message passing, while minimizing both hardware and software overhead. Each node in FLASH contains a microprocessor, a portion of the machine's global memory, a port to the interconnection network, an I/O interface, and a custom node controller called MAGIC. The MAGIC chip handles all communication both within the node and among nodes, using hardwired data paths for efficient data moveme ...

9 Design methodology management using graph grammars
Reid Baldwin, Moon Jung Chung
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(208.93 KB) Additional Information: full citation, references, index terms

10 Tools and strategies for dynamic verification: Systematic functional coverage metric synthesis from hierarchical temporal event relation graph
Young-Su Kwon, Young-Il Kim, Chong-Min Kyung
June 2004 **Proceedings of the 41st annual conference on Design automation**
Full text available: pdf(155.22 KB) Additional Information: full citation, abstract, references, index terms

Functional coverage is a technique for checking the completeness of test vectors in HDL simulation. Temporal events are used to monitor the sequence of events in the specification. In this paper, automatic generation of temporal events for functional coverage is proposed. The HiTER is the graph where nodes represent basic temporal properties or subgraph and edges represent time-shift value between two nodes. Hierarchical temporal events are generated by traversing HiTER such that invalid, or irr ...

Keywords: functional coverage, semi-formal verification, temporal event

11 PLI workshops: Trace analysis of Erlang programs
Thomas Arts, Lars-Åke Fredlund
December 2002 **ACM SIGPLAN Notices**, Volume 37 Issue 12

Full text available: pdf(139.00 KB) Additional Information: full citation, abstract, references

The paper reports on an experiment to provide the Erlang programming language with a tool package for convenient trace generation, collection and to support analysis of traces using a set of techniques. Due to the frequent use of state-based software design patterns in Erlang programming we can in many cases recover not only the events from a trace log, but also the program states causing these events. This makes it possible to obtain program models from execution traces. In our work we make use ...

12 The Stanford FLASH multiprocessor

Jeffrey Kuskin, David Ofelt, Mark Heinrich, John Heinlein, Richard Simoni, K. Gharachorloo, J. Chapin, D. Nakahira, J. Baxter, M. Horowitz, A. Gupta, M. Rosenblum, J. Hennessy

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: pdf(1.48 MB) Additional Information: full citation, references, index terms

13 Business-to-business interactions: issues and enabling technologies

B. Medjahed, B. Benatallah, A. Bouguettaya, A. H. H. Ngu, A. K. Elmagarmid

May 2003 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 12 Issue 1

Full text available: pdf(558.34 KB) Additional Information: full citation, abstract, index terms

Business-to-Business (B2B) technologies pre-date the Web. They have existed for at least as long as the Internet. B2B applications were among the first to take advantage of advances in computer networking. The Electronic Data Interchange (EDI) business standard is an illustration of such an early adoption of the advances in computer networking. The ubiquity and the affordability of the Web has made it possible for the masses of businesses to automate their B2B interactions. However, several issu ...

Keywords: B2B Interactions, Components, E-commerce, EDI, Web services, Workflows, XML

14 Approximate mean value analysis algorithms for queuing networks: existence, uniqueness, and convergence results

K. R. Pattipati, M. M. Kostreva, J. L. Teele

July 1990 **Journal of the ACM (JACM)**, Volume 37 Issue 3

Full text available: pdf(2.15 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper is concerned with the properties of nonlinear equations associated with the Scheweitzer-Bard (S-B) approximate mean value analysis (MVA) heuristic for closed product-form queuing networks. Three forms of nonlinear S-B approximate MVA equations in multiclass networks are distinguished: Schweitzer, minimal, and the nearly decoupled forms. The approximate MVA equations have enabled us to: (a) derive bounds on the approximate throughput; (b) prove the existence and uniqueness of the ...

15 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

16 Disco: running commodity operating systems on scalable multiprocessors

Edouard Bugnion, Scott Devine, Mendel Rosenblum

October 1997 **ACM SIGOPS Operating Systems Review , Proceedings of the sixteenth ACM symposium on Operating systems principles**, Volume 31 Issue 5

Full text available: pdf(2.30 MB) Additional Information: full citation, references, citings, index terms

17 Balancing performance and flexibility with hardware support for network architectures

Ilija Hadžić, Jonathan M. Smith

November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4

Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

18 Evaluating distributed functional languages for telecommunications software

J. H. Nyström, P. W. Trinder, D. J. King

August 2003 **Proceedings of the 2003 ACM SIGPLAN workshop on Erlang**

Full text available: pdf(182.87 KB) Additional Information: full citation, abstract, references

The distributed telecommunications sector not only requires minimal time to market, but also software that is reliable, available, maintainable and scalable. High level programming languages have the potential to reduce development time and improve maintainability due to their compact code size. Moreover reliability is improved by safe type systems and relatively easy verification.This paper outlines plans and initial results from a joint project between Motorola and Heriot-Watt University that ...

19 Disco: running commodity operating systems on scalable multiprocessors

Edouard Bugnion, Scott Devine, Kinshuk Govil, Mendel Rosenblum

November 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 4

Full text available: pdf(400.76 KB) Additional Information: full citation, abstract, references, citings, index terms, review

In this article we examine the problem of extending modern operating systems to run efficiently on large-scale shared-memory multiprocessors without a large implementation effort. Our approach brings back an idea popular in the 1970s: virtual machine monitors. We use virtual machines to run multiple commodity operating systems on a scalable multiprocessor. This solution addresses many of the challenges facing the system software for these machines. We demonstrate our approach with a prototy ...

Keywords: scalable multiprocessors, virtual machines

20 Clusters for nothing and nodes for free

Alexander Perry, Hoke Trammell, David Haynes
July 2004 **Linux Journal**, Volume 2004 Issue 123

Full text available: html(26.36 KB) Additional Information: full citation, abstract

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